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FORM PTO-1083		FEB 2 4 2003	C26						Case Do	ocket No. 1	5.49/60
In re the Application of Yoshikazu KASUYA Serial No.: 09/963,924		PADENTS		Group	Art Unit:	2814					
	6, 2001)	Examir	ner: Rao,	S.					
For: METHODS FO)						,		
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SEMICONDUC	TOR D	EVICES)							읖	
ASSISTANT COMMISS Washington, D.C. 20231		OF PATENTS								FEB 28 2003 ECHNOLOGY CENTER	RECEIVE
Sir:										CEN	
submitted.	us of thi	is application under	· 37 CFR	1.9 and 1	.27 has t				ified staten		
The fee has been calculat	ed as sh	own below:									
	AFTE	AINING		EST NO IOUSLY FOR	PRESE	NT A RATE	ADDIT		RATE	ADDIT. FEE	
TOTAL	22	MINUS	21	=	1	x	\$9	OR	x 18	\$ 18	
INDEP CLAIMS *	3	MINUS	5	=	0	X	\$42	OR	x 84	\$0	
FIRST PRESENT	ATION	OF MULTIPLE D	EP. CLA	AIM		+	\$	OR	+ 270		

Please charge Deposit Account No. 50-0585 the amount of \$ to cover the extension fee and also the amount of \$ to cover the claim fee. A duplicate copy of this sheet is enclosed.

TOTAL

A check in the amount of \$ ____ to cover the extension fee is enclosed.

X A check in the amount of \$ 18 to cover the filing fee for additional claims is enclosed.

<u>X</u> The Commissioner is hereby authorized to charge payment of the following fees associated with this communication or credit any overpayment to Deposit Account No. No. 50-0585. A duplicate of this sheet is enclosed.

<u>X</u> Any filing fees under 37 CFR 1.16 for the presentation of extra claims.

X Any patent application processing fees under 37 CFR 1.17.

Respectfully submitted,

Dated: February 21, 2003 Alan S. Raynes

Registration No. 39,809

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TOTAL \$ 18

I hereby certify that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231 on Feb. 21,2003.



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re the Application of)	ri C
Yoshikazu KASUYA) Group Art Unit: 2814	20 [
Serial No.: 09/963,924) Examiner: Rao, S.	~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~ ~
Filing Date: Sept. 26, 2001) Examiner: Rao, S.	
For: METHODS FOR MANUFACT		
SEMICONDUCTOR DEVICES	AND)	
SEMICONDUCTOR DEVICES) AMENDMENT	

Assistant Commissioner for Patents Washington, DC 20231

Dear Sirs:

In response to the Office Action dated Nov. 21, 2002, the response being due by Feb. 21, 2003, please enter and consider the following.

IN THE SPECIFICATION:

On page 1, please delete the first paragraph and insert the following in its place:

--Applicant hereby incorporates by reference Japanese Application No. 2000-292143, filed September 26, 2000, in its entirety. Applicant hereby incorporates by reference U.S. Application Serial No. 09/963,168 in its entirety. Applicant hereby incorporates by reference U.S. Application Serial No. 09/963,903 in its entirety.--

IN THE CLAIMS:

Please amend claims 1, 3 and 5-17 as follows:

rease amend claims 1, 3 and 3-17 as follows

1. (amended)

A method for manufacturing a semiconductor device, the method

comprising the steps of:

- (a) forming a gate dielectric layer;
- (b) forming a first conductive layer on the gate dielectric layer;

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